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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,763	09/17/2003	Kent A. Dickey	10002827-2	1746

7590 08/12/2005

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EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,763	DICKEY ET AL.	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *1-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-39* is/are rejected.

7)☒ Claim(s) *22,23,37,38 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Double Patenting

1. Claims 21, 22, 23, 26, and 29-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,651,193 B1. The body of the rejection can be found in the previous Office Action mailed February 18, 2005.

Claim Rejections - 35 USC § 112

2. In view of the Applicant's argument, the rejection of claim 23 under 35 USC § 112 has been withdrawn.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 21, 24-31, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillett, Jr. et al., U.S. Patent 6,295,585 B1.

Referring to claim 21:

a. In the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory (high performance coherent memory).

b. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of

Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (reading an error indication included in a packet, reflective of a current state of a unit; determining if said current state of said unit is in error mode). Further, in column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery.

c. In column 8, lines 31-55, Gillett, Jr. et al. disclose that the system operates normally unless the STAE bit is set (permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode).

d. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error (driving an error indicator to a subject processor if said current state of unit is in error mode).

e. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. Further, in column 14, lines 40-42, Gillett, Jr. et al. disclose that by halting data transmission from a faulty node, faulty data is not propagated to other nodes in the system (ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode).

Referring to claim 24, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said error indication in said packet is in the form of an error bit).

Referring to claim 25, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry (said error indication in said packet contained within a header of said packet).

Referring to claims 26 and 28, in column 10, lines 25-29, Gillett, Jr. et al. disclose that the hardware provides certain basic structural elements that ensure adequate software control of the structure, such as guaranteeing that order on the data link is preserved, providing loop-back capability, and terminating transmission to facilitate quick handling of errors (implementing a software recovery routine by said subject processor).

Referring to claim 27, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said reading step includes reading said error indication from an error bit).

Referring to claims 29 and 31, in the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory. Further, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some

point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set. Thus the error bit that is set is in response to an error in shared memory (setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area).

Referring to claim 30, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said error bit is provided as a fatal error bit).

Referring to claim 39, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry (means for transporting error indications together with data which is in error). Further, in Figure 8, Gillett, Jr. et al. disclose that the header is sent with the data. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error

(STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data). Further, in column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery.

Claim Rejections - 35 USC § 103

5. In view of the Applicant's argument, the rejection of claims 22, 23, 32-37, and 40 under 35 U.S.C. 103(a) as being unpatentable over Gillett, Jr. et al., U.S. Patent 6,295,585 B1, and further in view of Hornung, U.S. Patent 6,175,931 B1 has been withdrawn.

Allowable Subject Matter

6. Claim 40 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 22, 23, and 32-37 would be allowable if the double patenting rejection was overcome and if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed June 16, 2005 have been fully considered but they are not persuasive.

9. On page 6, under the section Rejection under 35 U.S.C. § 102, with reference to claim 21, the Applicant argues, "Claim 21 defines a method for providing a distributed high performance coherent memory with error containment that includes reading an error indication included in a data packet, reflective of a current state of a unit. Gillett does not disclose at least this limitation." The Examiner respectfully disagrees. In column 13, lines 36-40, Gillett, Jr. et al. disclose that the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet, to provide an error detection and recovery. Further, in column 13, lines 41-51 and in column 13 line 66 through column 14 line 7, Gillett discloses that the TPE bit and RPE bit indicates errors in the unit.

10. On page 6, under the section Rejection under 35 U.S.C. § 102, with reference to claim 39, the Applicant argues, "Claim 39 defines a system for error containment comprising means for transporting error indications together with data which is in error. Gillett does not disclose at least this limitation." The Examiner respectfully disagrees for at least the reasons given in paragraph 8 above.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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